REMARKS

Claims 1, 3, and 5-7 are currently amended, and claims 4, 36-95, 98-99, and 102-103 are canceled. Claims 36-95, 98-99, and 102-103 are canceled in that they correspond to non-elected subject matter. Applicant reserves the right to present claims 36-95, 98-99, and 102-103 in one or more divisional applications. Applicant respectfully submits that the amendments contained herein are fully supported by the Specification as originally filed and do not contain new matter.

Election/Restrictions

The above Office Action indicated that Applicant's election of Figures 1-2, claims 1-6, 9-10, 12-18, 20-22, 25-31, 33, 96-97, and 100-101 was treated as an election without traverse because Applicant did not distinctly and specifically point out the supposed errors in the restriction requirement (mailed on October 5, 2005). However, Applicant contends that the reply filed on October 20, 2005 distinctly and specifically points out the supposed errors in the restriction requirement.

In particular, the Examiner indicated in the restriction requirement that there were no generic claims. Applicant contended that elected claim 1 is generic to elected claims 2-6, 9-10, and 12-13 and non-elected claims 7-8 and 11, that elected claim 14 is generic to elected claims 15-18 and 20-22 and non-elected claims 19 and 23-24, and elected claim 25 is generic to elected claims 26-31 and 33 and non-elected claims 32 and 34-35. Therefore, upon allowance of claim 1, Applicant is entitled to consideration of non-elected claims 7-8 and 11, as provided by 37 C.F.R. § 1.141. Moreover, since claims 14 and 25 were indicated as allowed, Applicant respectfully requests that non-elected claims 19 and 23-24 and non-elected claims 32 and 34-35 be considered, as provided by 37 C.F.R. § 1.141.

Drawing Objections

The drawings were objected to under 37 CFR § 1.83(a). The Examiner indicated that the limitations of claims 4, 14, 21, 25, 96-97, and 100-101 must be shown or canceled from the claims. Applicant respectfully submits that the features of claims 4, 14, 21, 25, 96-97, and 100-101 are shown in the drawings.

Claim 4 is canceled, mooting the objection thereto. However, claim 1, as currently amended, includes the limitations of claim 4. Paragraphs [0016] and [0022] indicate that Figures 1 and 2 are cross-sectional views taken along substantially perpendicular planes of a multi-layer

memory array. Figure 1 illustrates a first contact 116 penetrating through each layer of memory material in a first plane, the plane of Figure 1, and Figure 2 illustrates a second contact 130 penetrating through each of the layers of memory material in a second plane, the plane of Figure 2, that is substantially perpendicular to the first plane, the plane of Figure 1, as per paragraphs [0016] and [0022]. Therefore, all of the features claim 4 included in currently amended claim 1 are shown in Figures 1 and 2, so the objection should be removed.

Paragraph [0038] indicates that for one embodiment, each layer 104 contains a NAND memory array 400, as shown in Figure 4, and paragraph [0043] indicates that for another embodiment, each layer 104 contains a NOR memory array 500, as shown in Figure 5. Note that layers 104 are shown in Figures 1 and 2 and correspond to the layers of memory material recited claims 14, 25, 96-97, and 100-101. Figure 1 illustrates a contact 116 passing through each layer 104 of memory material, and Figure 2 illustrates a contact 130 penetrating through each of the layers 104 of memory material, as recited in claims 14, 25, 96-97, and 100-101. Figures 4 and 5 each illustrate that a plurality of contacts 116 and 130 pass through each of the layers 104, as recited in claims 14, 25, 96-97, and 100-101, in that paragraphs [0038] and [0043] respectively indicate that Figures 4 and 5 correspond to each of the layers 104. Moreover, Figures 4 and 5, show that each of the layers 104 contain an array of memory cells arranged in rows and columns, as recited in claims 14, 25, 96-97, and 100-101. Figures 1 and 2 show each of layers 104 of memory material separated from each other by a dielectric material 106, as recited in claims 14, 25, 96-97, and 100-101.

Figure 5 illustrates contacts 116 in electrical communication with memory cells 506 of columns of memory cells 506, and contacts 130 in selective electrical communication with rows of memory cells 505, as recited in claims 14, 96, and 100. Figure 5 further illustrates a plurality of select transistors 170, with each select transistor 170 connected between a contact 130 and its respective row of memory cells, as recited in claims 14, 96, and 100. Figure 4 illustrates contacts 130 in electrical communication with memory cells rows of memory cells and contacts 116 in selective communication with columns of memory cells, as recited in claims 25, 97, and 101. Figure 4 further illustrates a plurality of select transistors 412, with each select transistor 412 connected between a contact 116 and its respective column of memory cells, as recited in claims 21, 25, 97, and 101.

Figure 4 shows a plurality of column lines 402 and a plurality of row lines 404, and Figure 5 shows a plurality of column lines 504 and a plurality of row lines 502. The column

lines in each of Figures 4 and 5 are respectively coupled to contacts 116, and the row lines in each of Figures 4 and 5 are respectively coupled to contacts 130. This means that each of the contacts 116 corresponds to a column line of each of the layers and each of the contacts 130 corresponds to a row line of each of the layers. Further, Figure 1 is a cross section of the multi-layer memory array along a column direction of Figure 4 or 5, as indicated by the contact 116, and Figure 2 is a cross section of the multi-layer memory array along a row direction of Figure 4 or 5, as indicated by the contact 130. Figure 1 illustrates a global bit line 112 in electrical communication with one of the contacts 116 of Figure 4 or 5, and Figure 2 illustrates a global row line 114 in electrical communication with one of the contacts 130 of Figure 4 or 5, as recited in claims 96-97 and 100-101. This means that there is a global bit line 112 for each contact 116 of Figure 4 or 5 and a global row line 114 for each row and contact 130 of Figure 4 or 5. Therefore, there are a plurality of global row lines and a plurality of global bit lines, as recited in claims 96-97 and 100-101.

Figure 6 illustrates a processor 620 connected to a memory device 602, as recited in claims 100 and 101. Figure 6 also shows row access circuitry 608 and column access circuitry 610. Although row access circuitry 608 is not specifically shown as connected to global row lines, to access rows of a memory array, original claims 96-97 and 100-101 described the connectivity, and, for clarity, Figure 6 leaves out certain details known to those skilled in the art. Similarly, although column access circuitry 610 is not specifically shown as connected to global bit lines, to access columns of a memory array, original claims 96-97 and 100-101 described the connectivity, and, for clarity, Figure 6 leaves out certain details known to those skilled in the art.

In view of the above, Applicant respectfully requests that the objection to the drawings under 37 CFR § 1.83(a) with respect to claims 4, 14, 21, 25, 96-97, and 100-101 be removed.

Claim Rejections Under 35 U.S.C. § 102

Claims 1 and 2 were rejected under 35 U.S.C. § 102(b) as being anticipated by Hilbert (U.S. Patent No. 6,377,504). Applicant respectfully traverses. Claim 1, as currently amended, is equivalent to writing claim 4 in its independent form in that claim 1, as currently amended, includes the limitation of claim 4, which depended directly therefrom. Therefore, claim 1 is allowable in that the Examiner indicated that claim 4 would be allowable if rewritten in independent form, as indicated below. Claim 2 depends from claim 1 and is thus allowable for at least the same reasons as claim 1. Therefore, claim 2 should be allowed.

Claim Rejections Under 35 U.S.C. § 103

Claims 9 and 13 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Hilbert (U.S. Patent No. 6,377,504) in view of Rowlandson et al. (U.S. Patent No. 6,636,442). Claims 10 and 12 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Hilbert (U.S. Patent No. 6,377,504) in view of Edwards et al. (U.S. Patent No. 6,937,248). Applicant respectfully traverses.

Claim 1, as currently amended, is patentably distinct from Hilbert. Moreover, Hilbert in combination with Rowlandson et al. fails to overcome the deficiencies of Hilbert with respect to claim 1. Therefore, claim 1 is allowable over Hilbert in view of Rowlandson et al. Hilbert in combination with Edwards et al. et al. fails to overcome the deficiencies of Hilbert with respect to claim 1. Therefore, claim 1 is allowable over Hilbert in view of Edwards et al. Claims 9-10 and 12-13 depend from claim 1 and are thus allowable for at least the same reasons as claim 1. Therefore, claims 9-10 and 12-13 should be allowed.

Allowable Subject Matter

Claims 3-6 were objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form, including all of the limitations of the base claim and any intervening claims. Claim 4 is canceled, mooting the objection thereto. Applicant has amended claim 3 as suggested by the Examiner. Applicant thus respectfully requests reconsideration and withdrawal of the objection, and allowance of claim 3. Claims 5-6 have not been rewritten. Claims 5-6 depend from claim 1 and are thus allowable for at least the same reasons as claim 1. Therefore, claims 5-6 should be allowed.

Applicant acknowledges that claims 14-18, 20-22, 25-31, 33, 96-97 and 100-101 were allowed.

CONCLUSION

In view of the above remarks, Applicant believes that the claims are in condition for allowance and respectfully requests a Notice of Allowance be issued in this case. If the Examiner has any questions regarding this application, please contact the undersigned at (612) 312-2208.

Respectfully submitted,

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